CapSense Express™ – Migrating from Firmware Rev 0x15 to Rev 0x1B

AN48303

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Associated Application Notes: AN47716, AN44208, AN44207, AN42137, AN48430, AN2352

Application Note Abstract

This application note discusses the compatibility issues that need to be considered before migrating from CapSense Express firmware revision 0x15 to 0x1B. In August 2008, all Cypress inventories were rotated to the new CapSense Express firmware (0x1B). Rotation of all distribution inventories is planned to be completed by October 2008.

Introduction

CapSense Express supports up to 10 IOs that can be configured as capacitive sensing inputs or digital GPIOs. These configurable IOs are used for operations such as, interrupt, wakeup line, and PWM output.

Firmware Rev 0x1B provides an enhanced performance and introduces several features, which require particular attention when migrating from an existing project that uses Rev 0x15.

The following two aspects need to be considered before migrating to Rev 0x1B:

- Host controller firmware code
- Use of CapSense Express configuration files generated with PSoC Express 3.0

Note In WW35 2008, all Cypress inventories were rotated to the new CapSense Express firmware (0x1B). The distribution inventories are planned to be rotated by WW42 2008.

Summary of Enhancements

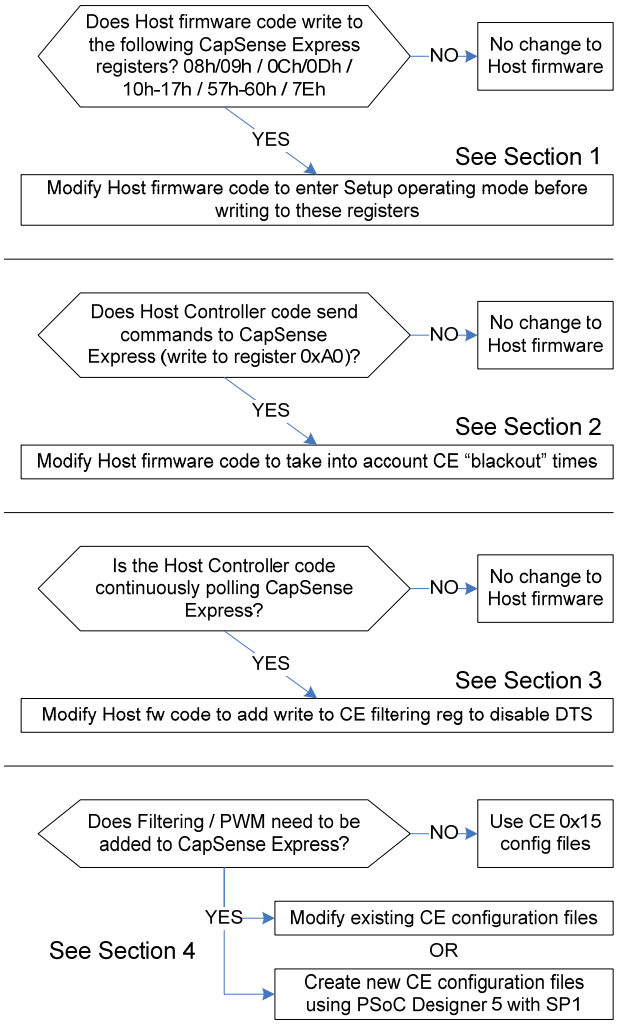
CapSense Express Firmware revision 0x1B includes the following enhancements:

- CapSense signal filtering (averaging)
- PWM output for LED dimming control (CY8C20110)
- Significant reduction of I^2C ACK time in Normal operating mode (worst case is less than 140 µs).
- I^2C bus is not stalled during the execution of flash write commands. The bus is released within 100 µs.

These enhancements are not explained in detail in this application note. Instead, this application note deals with the effects of the enhancements on the register and device accessibility. Previously developed Host communication schemes used with firmware revision 0x15 may be affected.

Migration Process Overview

Figure 1. Flowchart of the Migration Process



1. Register Map and Access in Setup and Normal Modes

One of the measures implemented to optimize the I^2C ACK response time is to differentiate between Setup operating mode and Normal operating mode. This is done so that registers in Normal operating mode that require long processing times cannot be written. This optimization leads to short "optimized" ACK times in Normal operating mode, and longer ACK times in Setup operating mode.

In CapSense Express firmware revision 0x1B, some registers, previously available for W/R access in Normal operating mode, are now Read Only. Register access in Setup operating mode is always W/R for all writeable registers.

Table 1 lists the CapSense Express register map summary with the access type. The new Read Only registers in Normal operating mode are indicated by a bold style and an asterisk (*). For the entire register map, refer to CY8C201XX Register Reference Guide.

Table 1. Register Map Summary with Access Type

Address	Register	Setup Access	Normal Access
00/01h	Input	Read	Read
02/03h	Latched Status	Read	Read
04/05h	Output	Write	Write
06/07h	CapSense Input	Write/Read	Read
08/09h*	**Enabled GPIO***	**Write/Read***	**Read***
0A/0Bh	Inversion	Write/Read	Write/Read
0C/0Dh*	**Interrupt Mask***	**Write/Read***	**Read***
0E/0Fh	Status Hold Mask	Write/Read	Write/Read
10-13h*	**Drive Modes***	**Write/Read***	**Read***
14-17h*	**Drive Modes***	**Write/Read***	**Read***
18/19h	PWM enable	Write/Read	Write/Read
1Ah	PWM configuration	Write/Read	Write/Read
1Bh	PWM delay	Write/Read	Write/Read
1C-34h	GP00-04 - Operation Settings	Write/Read	Write/Read
35-4 Dh	GP10-14 - Operation Settings	Write/Read	Write/Read
4Eh	Noise Threshold	Write/Read	Write/Read
4Fh	Baseline Update Th	Write/Read	Write/Read
50h	Settling Time	Write/Read	Read
51h	Ext C, Sns Rst, Clk Sel	Write/Read	Read
52h	Hysteresis	Write/Read	Write/Read
53h	Debounce	Write/Read	Write/Read
54h	Negative Noise Th	Write/Read	Write/Read
55h	Low Baseline Reset	Write/Read	Write/Read
56h	Filtering	Write/Read	Write/Read
57-60h*	**GPXX - Scan Position***	**Write/Read***	**Read***
61-6Ah	GPXX - Finger Th	Write/Read	Write/Read
6B-74h	GPXX – IDAC setting	Write/Read	Write/Read
75h	Slider Configuration	Write/Read	Write/Read
76h	Reserved	Reserved	Reserved

Address	Register	Setup Access	Normal Access
77h	Slider Resolution MSB	Write/Read	Write/Read
78h	Slider Resolution LSB	Write/Read	Write/Read
79h	I2C Dev Lock	Write/Read	Write/Read
7A/7 Bh	Device ID / Status	Read	Read
7Ch	I2C address, I2CDM	Write/Read	Write/Read
7Dh	Reserved	Reserved	Reserved
7 Eh*	**Sleep Control Pin***	**Write/Read***	**Read***
7 Fh	Sleep Control	Write/Read	Write/Read
80h	Stay-Awake Counter	Write/Read	Write/Read
81h	Button Select	Write/Read	Write/Read
82h	Baseline	Read	Read
84h	Sensor Difference	Read	Read
86h	Result	Read	Read
88h	Sensor On Mask	Read	Read
8 Ah	Centroid position	Read	Read
8 Ch	Centroid Peak	Read	Read
A0h	Command Register	Write	Write

For more information on I^2C ACK response times in Normal and Setup operating modes, refer to the application note AN44208 "I^2C Communication Timing Analysis".

Host Controller Firmware Considerations for Register Access Changes

Changes to the registers' access type in "Normal operating mode" affect the existing Host controller firmware code, only if the modified registers are accessed for write.

To ensure successful writing to the modified registers, first set up CapSense Express to Setup operational mode. The Host controller can use the following API described in AN44207:

```
CE_EnterCommandCode(SETUP_OPERATION_MODE)
```

After the relevant registers are modified, set back CapSense Express to Normal operating mode using the following API:

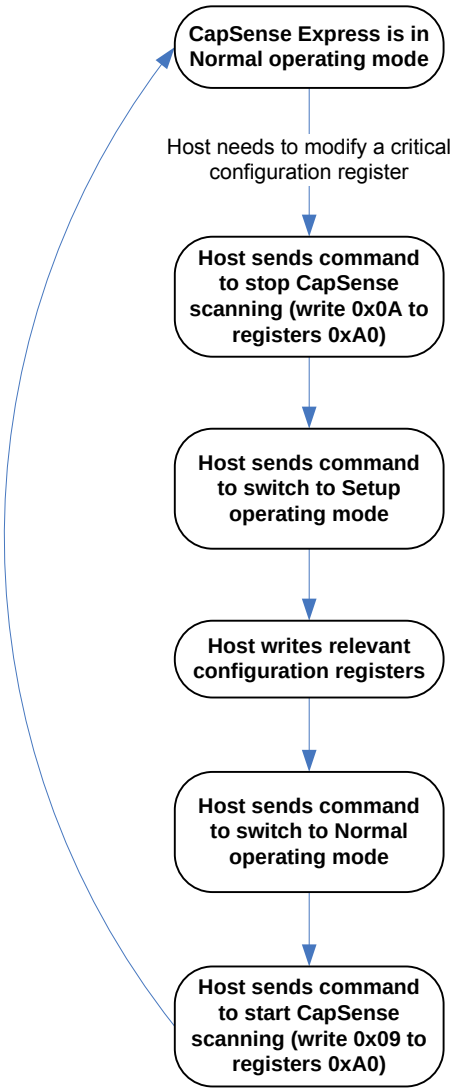
```
CE_EnterCommandCode(NORMAL_OPERATION_MODE)
```

Note that the registers with Read Only access in Normal mode are limited to only configuration registers. These registers are usually accessed only during initial configuration and debug.

The acknowledgement time in Setup operating mode can be maintained to match the time taken in Normal operating mode. To achieve this, first stop the CapSense scanning before switching to Setup operating mode. Then, restart CapSense scanning after moving to Normal operating mode.

Figure 2 shows an example of a flow used to change registers (that are ReadOnly in Normal mode) in Setup operating mode, with close to optimal ACK response time.

Figure 2. Changing Registers in Setup Operating Mode



2. Command Execution

Commands are executed in CapSense Express by writing the command code to register 0xA0.

In CapSense Express firmware release 0x15, the I^2C bus is stalled until the execution of the command is completed. This results in very long ACK times (approximately, 100 ms).

In the implementation with firmware release 0x1B, the I^2C bus is released within 100 µs (in Normal mode). After the bus is released (ACK is sent), the CapSense Express device cannot be accessed for the time needed to execute the command. The device appears as nonexistent to the Host device (disconnected from the I^2C bus). The time during which the device cannot be accessed is called "blackout" time.

Table 2 lists the typical blackout time for the various commands.

Table 2. Register Map Summary with Access Type

Cmd	Description	Mode	Blackout after ACK
00h	Get FW rev.	Setup/Normal	0 s
01h	Store current config to flash	Setup/Normal	120 ms
02h	Restore factory config	Setup/Normal	120 ms
03h	Write POR defaults	Setup/Normal	120 ms
04h	Read POR defaults	Setup/Normal	5 ms
05h	Read current config	Setup/Normal	5 ms
06h	Reconfig device (POR)	Setup	5 ms
07h	Normal mode	Setup/Normal	0s
08h	Setup mode	Setup/Normal	0s
09h	Start CapSense scan	Setup/Normal	10 ms
0Ah	Stop CapSense scan	Setup/Normal	5 ms
0Bh	Get CapSense scan status	Setup/Normal	0s

Note POR = Power On Reset.

Trying to access the device immediately after the I^2C bus is released (ACK is sent) does not interfere with other devices connected to the I^2C bus of the system. CapSense Express does not respond to I^2C requests, which effectively NAKs its address byte.

Host Controller Firmware Considerations for Commands Execution

When sending a command to CapSense Express, the Host controller receives an ACK within 100 µs. This enables communication to other devices on the same I^2C bus.

However, CapSense Express cannot be accessed during the blackout time, as listed in Table 2.

As a result, the Host controller either waits for a fixed time before reaccessing CapSense Express, or periodically polls CapSense Express until a response is received. After a response is received (for example, an ACK after sending the CapSense Express device address), the Host knows that CapSense Express has executed the command and is ready for a new I^2C transaction.

3. Filtering and PWM Output Functionalities

The additional features implemented in CapSense Express firmware revision 0x1B do not affect any other functionality already existing in firmware revision 0x15.

However, there is one exception. You must disable a filtering mode in case of an application in which the Host continuously communicates with CapSense Express.

If an I^2C transaction with CapSense Express is concurrent for any amount of time with a capacitance scan, the sensing engine by default discards the acquired sample. As a result, the noise introduced by the I^2C communication does not affect the sensor status (ON or OFF) decision process.

In case of a continuous Host communication with CapSense Express, there is a risk that a very high percentage of the acquired sensors' samples are discarded if this filter is enabled. This could result in a perceived slow response of CapSense Express to finger touch events.

To disable this type of filter ("I^2C Drop The Sample" or DTS), clear the appropriate bit in CapSense Express register 0x56 (filtering configuration).

If this filter is disabled, enable the averaging filter, so that noise can still be controlled, and the sensor status decision process robustness is not affected.

4. Using CapSense Express Configuration Files

PSoC Express 3.0 does not support CapSense Express firmware revision 0x1B. However, flash configuration files generated for firmware revision 0x15 can be used without any change to configure 0x1B parts.

Since firmware revision 0x15 does not support PWM output and filtering, the registers in the configuration files for 0x15 are set to 0x00. To take advantage of the new features:

- Change the configuration files manually
- Create new configuration files using PSoC Designer 5 with Service Pack 1.

With the first option, after customization of the configuration files, the Cypress I^2C-USB bridge (hardware and software) is used to load the configuration onto CapSense Express.

With the second option, no further custom step is required because both CapSense Express firmware revisions 0x1B and 0x15 are fully supported.

Note that PSoC Designer 5 contains all the familiar PSoC Express 3.0 functionality embedded within the System-Level editor. All CapSense Express designs are created and edited as system level projects.

Download PSoC Designer 5 and Service Pack 1 at the following link: http://www.cypress.com/?id=1147.

Customizing Configuration Files created for Firmware Revision 0x15

This section describes customizing the configuration files. This process is needed only to enable PWM output and filtering features, which are available in firmware revision 0x1B. The configuration files generated with PSoC Express 3.0 for firmware revision 0x15 is used in this process. PSoC Express no longer supports CapSense Express. You need to migrate to at least PSoC Designer 5.0 SP1.

For each CapSense Express project, two configuration files are generated by the software tool:

- *project_name*_config_through_regs.iic
- *project_name*_config_through_flash.iic

These files contain the I²C data streams and command sequences to configure CapSense Express. Use either of these options to configure the part. The first file is a 'verbose' mode, and the second file is a 'single command' mode.

Verbose Mode: Customizing project_name_config_through_regs.iic

This configuration file is typically in the following form (line numbers are added for reference):

```
line 1:   w 00 79 3C A5 69
line 2:   w 00 7C 80
line 3:   w 00 79 96 5A C3
line 4:   w 00 A0 08
line 5:   w 00 08 00 00
line 6:   w 00 06 04 18 1B 07 0B 07 00 00 1F
1F 00 0B 00 10 00 07 00 00
line 7:   w 00 04 10 00
line 8:   w 00 1C E8 04 00 10 18 E1 04 10 10
00 00 00 00 00 00 E8 00 10 14 08 00 00 00
00 00 E1 00 18 10 00 E1 04 08 10 00 E8 00
08 14 10 00 00 00 00 00 00 00 00 00 00
line 9:   w 00 4E 28 64 A0 40 0A 03 14 14 00
line 10:  w 00 57 00 00 00 00 00 00 00 00 00
00 00 00 64 00 00 00 00 00 64 64 00 00 09
00 00 00 00 00 0B 0A
line 11:  w 00 7E 00 20 00
line 12:  w 00 A0 01
line 13:  w 00 A0 06
```

The 'w' in each line indicates an I²C write operation. The '00' after the 'w' is the CapSense Express I²C device address. The hex value following '00' is the CapSense Express register address for the write operation, and the subsequent hex values are the data. A brief explanation of the lines follows:

line 1: Unlock I²C address register
line 2: Set I²C address to 0x00 and I²C pin drive mode to 'Open Drain'
line 3: Lock I²C address register
line 4: Enter Setup operating mode
line 5: Start by disabling all GPIOs
line 6: Enable CapSense pins, GPIO, set inversion, drive modes,…
line 7: Set outputs
line 8: Configure logic operations
line 9: Set global CapSense parameters
line 10: Set sensors parameters
line 11: Sleep configuration
line 12: Store current configuration to flash
line 13: Reset the part

For parts with support for slider, an extra line is present to configure the slider.

To add configuration commands for PWM output and filtering, add two lines before line 11 (sleep configuration):

```
w 00 18 WW XX YY ZZ
w 00 56 KK
```

Where:

```
WW = PWM Enable Port 0
XX = PWM Enable Port 1
YY = PWM Configuration
ZZ = PWM Delay
KK = Filtering configuration
```

Single Command: Customizing project_name_config_through_flash.iic

This configuration file is in the following form:

```
w 00 A0 03 10 00 04 18 1B 07 0B 07 00 00 1F
1F 00 0B 00 10 00 07 00 00 00 00 00 00 E8
04 00 10 18 E1 04 10 10 00 00 00 00 00 00
E8 00 10 14 08 00 00 00 00 00 E1 00 18 10
00 E1 04 08 10 00 E8 00 08 14 10 00 00 00
00 00 00 00 00 00 00 28 64 A0 40 0A 03 14
14 00 00 00 00 00 00 00 00 00 00 00 00 00
64 00 00 00 00 00 64 64 00 00 09 00 00 00
00 00 0B 0A 00 00 00 00 80 23 00 20 00 5F
```

It consists of a single I²C write command (`w 00 A0 03`) followed by 122 bytes (highlighted in gray), and an error check value (`5F`).

The error check value is calculated as the XOR of all the previous 122 configuration bytes.

To add configuration parameters for PWM output and filtering, the following steps are needed:

- Change 4 bytes starting from byte 21 (PWM settings)
- Change byte 83 (Filtering settings)
- Recalculate the error check value (XOR of the previous 122 bytes)

After the file is customized, load the configuration on CapSense Express using the Cypress I²C-USB bridge.

Summary

Migrating existing configurations developed for CapSense Express products with firmware revision 0x15 to products with firmware revision 0x1B requires a review of the code developed for the Host microcontroller.

You can customize the CapSense Express configuration files generated with PSoC Express 3.0 to take advantage of the PWM and filtering features. However, PSoC Designer 5.0 with Service Pack 1 supports all the new features and enhancements introduced with firmware revision 0x1B.

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